

http://www.bits-pilani.ac.in/hyderabad/EEE/Home

## Ph.D. Admission in II Semester 2018 - 2019

(http://www.bitsadmission.com/phmain.aspx)

## 1. Department plan to admit student under:

- a. Full Time students: student who will devote full-time on PhD work.
- b. **Part-time Students**: Candidates working in organizations situated close to the campus will be admitted under this scheme. Students will have to complete required course work similar to full-time students as specified by the Department Research Committee (DRC). They will not be entitled for any assistantship from the Institute.

## 2. Eligibility for admission

- a. Essential Input criteria: As per Ph.D advertisement given in general information link
- **b. Shortlisting criteria** (for interview, there is *no written test* for EEE department):

Full time	Part time	
<ul> <li>M.E. / M.Tech (or equivalent) in Electrical / Electronics / Instrumentation or related areas (only interview for admission)</li> <li>A candidate must have 60% (or CGPA 6/10) during UG &amp; PG programmes</li> <li>B.E. / B.Tech (or equivalent) in Electrical / Electronics / Instrumentation or related area with exceptional academic background and research / industrial experience may be considered (interview for admission will be conducted for the candidates who will clear the written test)</li> <li>Openings are available in the selected areas</li> <li>Calling for written test/ interview will be at the discretion of the Department Research Committee</li> </ul>	<ul> <li>M.E. / M.Tech (or equivalent) in Electrical / Electronics / Instrumentation or related areas (only interview for admission)</li> <li>A candidate must have 60% (or CGPA 6/10) during UG &amp; PG programmes</li> <li>B.E. / B.Tech (or equivalent) in Electrical / Electronics / Instrumentation or related area with exceptional academic background and research / industrial experience may be considered (interview for admission will be conducted for the candidates who will clear the written test)</li> <li>Openings are available in the selected areas only</li> <li>Calling for written test/ interview will be at the discretion of the Department Research Committee</li> </ul>	

## 3. Area(s) of Ph D admission in the II Semester 2017-18 ( $\sqrt{\rightarrow}$ available PhD positions)

Area	FT	PT
Low power Arithmetic Circuits		
Power Systems & Power Electronics		V
Optical Communication, Optical MEMS		
Microwave Engineering		√
Embedded Systems		
MEMS / Microfluidics / Nanotechnology	V	
Nanoelectronic devices and circuits	V	
VLSI	V	√
Instrumentation and Sensors	V	
Digital Signal Processing	√	